WHAT IS CLAIMED IS:

1. A method of recovering a clock and data from a data signal comprising:

receiving the data signal having a first data rate;

receiving a clock signal having a first clock frequency, and alternating between a first level and a second level;

storing the data signal when the clock signal alternates from the first level to the second level, and providing the stored data signal as a first signal a first amount of time later;

storing the first signal when the clock signal alternates from the first level to the second level, and providing the stored first signal as a second signal a second amount of time later;

providing a third signal by delaying the first signal for a third amount of time;

storing the third signal when the clock signal alternates from the second level to the first level, and providing the stored third signal as a fourth signal a fourth amount of time later;

providing a fifth signal by delaying the data signal a fifth amount of time;

providing an error signal by taking the exclusive-OR of the first signal and the fifth signal; and

providing a reference signal by taking the exclusive-OR of the second signal and the fourth signal, wherein the first data rate is equal to the first clock frequency.

2. The method of claim 1 further comprising:

applying the error signal and the reference signal to a loop filter to generate a loop filter output.

3. The method of claim 2 wherein the storing the data signal is done by a first flip-flop, the storing the first signal is done by a third flip-flop, and storing the third signal is done by a second flip-flop.

4. The method of claim 3 wherein the providing the error signal and providing the reference signal is done by exclusive-OR gates.

5. The method of claim 1 wherein the first delay, the second delay, the fourth delay, and the fifth delay are approximately equal and the third delay is longer than the first delay.

6. The method of claim 5 wherein the third delay is approximately one-half the reciprocal of the first clock frequency.

7. An apparatus for recovering data from a received data signal comprising:

a first storage device configured to generate a first signal by receiving and storing the received data signal;

a second storage device configured to generate a second signal by receiving and storing the first signal;

a first delay block configured to generate a third signal by delaying the first signal;

a third storage device configured to generate a fourth signal by receiving and storing the third signal;

a second delay block configured to generate a fifth signal by delaying the received data signal;

a first logic gate configured to perform an exclusive-OR of the second and fourth signals; and

a second logic gate configured to perform an exclusive-OR of the first and fifth signals,

wherein when the first storage device stores the received data, the second storage device stores the first signal, and the third storage device does not store the third signal, and when the third storage device stores the third signal, the first storage device does not store the received data, and the second storage device does not store the first signal.

8. The apparatus of claim 7 wherein the first storage device stores the received data signal on falling edges of the clock, the second storage device stores the first signal on the falling edges of the clock, and the third storage device stores the third signal on the rising edges of the clock.

9. The apparatus of claim 8 wherein a delay through the second delay block is approximately equal to a clock-to-Q delay of the first storage element.

10. The apparatus of claim 9 wherein a delay through the first delay block is approximately equal to the time between a rising edge of the clock signal and a falling edge of the clock signal.

11. An apparatus for recovering data from a received data signal comprising:

a first flip-flop having a data input coupled to a first data input port, and a clock input coupled to a first clock port;

a second flip-flop having a data input coupled an output of the first flip-flop, and a clock input coupled to the first clock port;

a first delay element having an input coupled to the output of the first flip-flop;

a third flip-flop having a data input coupled to an output of the first delay element, and a clock input coupled to a second clock port;

a second delay element having an input coupled to the first data input port;

a first exclusive-OR gate having a first input coupled to the output of the second flip-flop, and a second input coupled to an output of the third flip-flop; and

a second exclusive-OR gate having a first input coupled to the output of the first flip-flop and a second input coupled the second delay element,

wherein the signal at the second clock port is the complement of the signal at the first clock port.

12. The apparatus of claim 11 wherein the first data input port is configured to receive a differential signal.

13. The apparatus of claim 12 wherein the first clock port is configured to receive a differential signal.

14. The apparatus of claim 13 wherein the first exclusive OR gate provides a reference signal, and the second exclusive OR gate provides an error signal.

15. An optical receiver comprising the apparatus of claim 11.

16. An optical transceiver comprising:

an optical transmitter; and

the optical receiver of claim 15 coupled to the optical transmitter.

17. A system for receiving and transmitting optical signals comprising:
a light emitting diode, configured to transmit optical signals;
a transmitter coupled to the light emitting diode;
a photo-diode, configured to receive optical signals;
a receive amplifier coupled to the photo-diode;
the apparatus of claim 11 coupled to the receive amplifier; and
a media access controller coupled to the apparatus of claim 11.

18. A method of modifying a signal path comprising an output of a first flip-flop coupled to an input of a second flip-flop and the output of the first flip-flop and an output of the second flip-flop coupled to a logic gate, the flip-flops clocked on consecutive transitions of a clock signal, the method comprising:

inserting a delay element between the output of the first flip-flop and the input of the second flip-flop, wherein a delay through the delay element is greater than a duration between consecutive transitions of the clock signal, less a clock-to-Q delay for the first flip-flop, and plus a hold time for the second flip-flop; and

inserting a third flip-flop between the first flip-flop and the logic gate, an input of the third flip flop coupled to the output of the first flip-flop, and an output of the third flip-flop coupled to the logic gate.

19. The method of claim 18 wherein the delay through the delay element is less than a duration between three consecutive edges of the clock signal, less the clock-to-Q delay for the first flip-flop, less a set-up time for the second flip-flop.

20. The method of claim 19 wherein the logic gate is an XOR gate.